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	Application No.	Applicant(s)	G,
Nation of Allowahility	10/024,103	MARUOKA, MICHIA	AKI
Notice of Allowability	Examiner	Art Unit	j
	Khiem D Nguyen	2823	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to <u>06/08/04</u> .			
2. The allowed claim(s) is/are 10 and 12-20.			
3. A The drawings filed on 17 December 2001 are accepted by	the Examiner.		
 4. Acknowledgment is made of a claim for foreign priority ur a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 	e been received. e been received in Application No		tion from the
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		complying with the rec	quirements
5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give			OTICE OF
6. CORRECTED DRAWINGS (as "replacement sheets") mus	st be submitted.		
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached			
1) hereto or 2) to Paper No./Mail Date			
(b) including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in the C	Office action of	
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			back) of
7. DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT			Note the
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date	5. ☐ Notice of Informal F 6. ☐ Interview Summary Paper No./Mail Da 7. ☐ Examiner's Amend	r (PTO-413), tle ment/Comment	
of Biological Material	9. 🗍 Other		

DETAILED ACTION

Allowable Subject Matter

Claims 10 and 12-20 are allowed.

Reasons For Allowance

The following is a statement of reasons for the indication of allowable subject matter: The prior art taken alone or in combination neither discloses nor makes obvious the instant process of claims as a whole. Specifically, the prior art of record, Lee (U.S. Patent 6,597,032) discloses a semiconductor device having a bonding pad electrode of a multi-layer structure, the semiconductor device comprising (col. 3, line 63 to col. 5, line 29 and FIGS. 1-4e): a semiconductor substrate (FIG. 4d: 100); a lower electrode layer (FIG. 4d: 108 a and 108b) formed on the semiconductor substrate; a cover insulating film (FIG. 4d: 110 and 114) formed on the lower electrode layer (col. 4, lines 26-39), wherein the cover insulating film has an opening (FIG. 4d: h2 and h3) for exposing at least a portion of the lower electrode layer (col. 4, lines 40-61), a step portion is provided at a side wall of the opening of the cover insulating film (FIGS. 4d-e), the size of the opening at the upside portion of a step surface of the step portion (opening at layer 114) is larger than the size of the opening at the downside portion of the step surface (opening at layer 110); and an upper electrode layer (FIG. 4d: 118a and 118b) formed on the portion of the lower electrode layer exposed via the opening, and the upper electrode layer overlaps the step surface of step portion (col. 5, lines 3-29) but fails to teach or suggest the Applicant's steps of wherein the forming an opening in the cover insulating film to expose at least a portion of the lower electrode layer comprises: forming a photo resist

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film having a first opening on said cover insulating film; and isotropically etching the cover insulating film by using the photo resist film as an etching mask, wherein the cover insulating film is side-etched with respect to the first opening of the photo resist film; wherein the forming an upper electrode layer on the portion of the lower electrode layer exposed via the opening is performed by using a lift-off method in which the photo resist film is used as a mask as recited in the currently amended independent claim 10, lines 14-22.

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Moreover, the prior art of record also does not explicitly disclose the step of wherein the cover insulating film comprises a silicon nitride film and a PSG film; wherein forming the cover insulating film on the lower electrode layer comprises: forming the silicon nitride film on the lower electrode layer; and forming the PSG film on the silicon nitride film, wherein forming an opening in the cover insulating film to expose at least a portion of the lower electrode layer comprises: forming a photo resist film having a first opening on the PSG film; isotropically etching the PSG film by using the photo resist film as an etching mask to form a second opening in the PSG film, wherein at least a portion of the silicon nitride film is exposed at the bottom portion of the second opening, and the PSG film is side-etched with respect to the first opening of the photo resist film; and plasma etching the silicon nitride film by using the photo resist film as an etching mask to form a third opening in the silicon nitride film, wherein at least a portion of the lower electrode layer is exposed at the bottom portion of the third opening, the third opening is smaller than the second opening, and the step surface of the step portion is formed by the upper surface portion of the silicon nitride film exposed via the second

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opening of the PSG film; and wherein forming an upper electrode layer on the portion of the lower electrode layer exposed via opening of the cover insulating film comprises: depositing a material to be the upper electrode layer on the exposed portion of the lower electrode layer, at least a portion of the step surface and the photo resist film; and removing a portion of the material deposited on the photo resist film by using a lift-off method, wherein portions of the material deposited on the exposed portion of the lower electrode layer and on the step portion are not removed, thereby the upper electrode layer is formed as recited in the currently amended independent claim 12, lines 14-38; currently amended independent claim 13, lines 14-40; and currently amended independent claim 14, lines 14-37.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N. August 30th, 2004

W. DAVID COLEMAN PRIMARY EXAMINER